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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,493	01/30/2001	David W. Duemler	D6570-00003	1363

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EXAMINER	
JOSEPH, THOMAS J	

ART UNIT	PAPER NUMBER
2174	

DATE MAILED: 11/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/772,493	DUEMLER, DAVID W.	
	Examiner	Art Unit	
	Thomas J Joseph	2174	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *23-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1 - 22, drawn to a user interface, classified in class 345, subclass 805.

   II. Claims 23 - 48, drawn to a program logic controller, classified in class 700, subclass 18.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a GUI for viewing contents and programming the program logic controller while invention II depicts the program logic controller itself. See MPEP § 806.05(d).

3. During a telephone conversation with 10-27-2003 Joseph A. Powers, Attorney for the Applicant on 10-27-2003, a provisional election was made without traverse to prosecute the invention of group I, claims 1 – 22. Applicant when replying to this Office action must make affirmation of this election. Claims 23 – 48 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 9, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 5,917,483) and Pasqali (US 6,535,882).

Claims 1, 9, 17, and 20:

Duncan et al. (US 5,917,483) teaches a method, apparatus, computer readable medium, and computer data signal for programming a programmable logic controller (col. 3, lines 30 – 40). All software requires a method, apparatus, computer readable medium, and computer data signal for programming a programmable logic controller. Duncan teaches a programmable logic controller including a plurality of inputs and a plurality of outputs (col. 3, lines 30 – 40). Duncan teaches a programmable logic controller directing a process through output signals at said outputs in response to input signals at said inputs (col. 3, lines 30 – 40). Duncan teaches displaying a user on a monitor a graphical data entry user interface (UI) for a plurality of sequential steps, said graphical data entry a user interface representing respective inputs to be monitored by said programmable logic controller at each of said sequential steps and respective outputs to be initiated by said programmable logic controller at respective ones of said sequential steps (col. 3, lines 30 – 40). Duncan fails to teach monitoring sequential steps and identifying at least one output selected by said user to be initiated for said at least one of said sequential steps.

Pasqali (US 6,535,882) teaches receiving via said graphical data entry user interface, an identification of at least one input selected by said user to be monitored for

at least one of said sequential steps and an identification of at least one output selected by said user to be initiated for said at least one of said sequential steps (col. 12, lines 1 – 25). Pasqali teaches converting said identification of said at least one input selected by said user into an input control data table, said input control data table including a plurality of input control data elements (col. 12, lines 1 – 25). Pasqali teaches input control data element corresponding to a respective one of said plurality of sequential steps (col. 12, lines 1 – 25). Pasqali teaches a respective one of said input control data elements representing said at least one input selected by said user (col. 12, lines 1 – 25). Pasqali teaches converting said identification of said at least one output selected by said user into an output data table (col. 11, lines 39 – 56). Pasqali teaches a plurality of output data elements each of said output data elements corresponding to a respective one of said plurality of sequential steps, a respective one of said output data elements representing said at least one output selected by said user (col. 11, lines 39 – 56).

It would have been obvious to one with ordinary skill in the art at the time of the invention to combine monitoring sequential steps and identifying at least one output selected by said user to be initiated for said at least one of said sequential steps taught by Pasquali with the logic control system disclosed by Duncan. Doing so enables step-by-step processing of the said logic control system.

6. Claims 2 – 5, 8, 10 – 13, 16, 18, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 5,917,483) and Pasqali

(US 6,535,882) as applied to claims 1, 9, 17, and 20 above, and further in view of Paraghamian et al (US 4,358,275).

Claims 2, 10, 18, and 21:

Duncan and Pasquali fail to teach a graphical data entry user interface including a timer enabling command option for each of said plurality of sequential steps and a timer value option for each said plurality of sequential steps. Paraghamian et al (US 4,358,275) teaches graphical data entry user interface including a timer enabling command option for each of said plurality of sequential steps and a timer value option for each said plurality of sequential steps (col. 5, lines 35 – 67). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine a user interface for graphical data entries that include a timer enabling command option for each of said plurality of sequential steps and a timer value option for each said plurality of sequential steps taught by Paraghamian with the logic control system disclosed by Duncan and Pasquali. Doing so enables the control of the processing speed.

Claims 3, 11, 19, and 22:

Paraghamian teaches receiving via said graphical data entry user interface, a selection by said user of a timer enabling command for at least one of said plurality of sequential steps (col. 5, lines 35 – 67). Paraghamian teaches receiving via said graphical data entry user interface, a selection by said user for a timer value for said one of said plurality of sequential steps (col. 5, lines 35 – 67). Paraghamian teaches creating a timer value data table including at least one timer value data element, said timer value data element representing said timer value (col. 5, lines 35 – 67).

Paraghamian teaches a respective one of said input control data elements representing said the timer enabling command for said one of said sequential steps (col. 5, lines 35 – 67).

Claims 4 and 12:

Paraghamian teaches an input control data element including a plurality of bits, a subset of said plurality of bits representing individual inputs of said programmable logic controller and at least a remaining one of said plurality of bits representing said timer enable command (col. 5, lines 35 – 67).

Claims 5 and 13:

Duncan and Pasquali fails to teach an input control data element including a plurality of bits and a subset of said plurality of bits representing individual inputs of said programmable logic controller. Paraghamian teaches an input control data element that includes a plurality of bits and a subset of said plurality of bits representing individual inputs of said programmable logic controller (col. 5, lines 35 – 67). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine an input control data element including a plurality of bits and a subset of said plurality of bits representing individual inputs of said programmable logic controller taught by Paraghamian with the logic control system disclosed by Duncan and Pasquali. Doing so enable tracking of data being processed.

Claims 8 and 16:

Duncan and Pasquali fails to teach Duncan and Pasquali fails to teach a subset of said plurality of bits representing individual outputs of said programmable logic

controller. Paraghamian teaches output data element including a plurality of bits (col. 5, lines 35 – 67). Paraghamian teaches a subset of said plurality of bits representing individual outputs of said programmable logic controller (col. 5, lines 35 – 67). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine a subset of said plurality of bits representing individual outputs of said programmable logic controller taught by Paraghamian with the logic control system disclosed by Duncan and Pasquali. Doing so enables the creation of output areas for producing program output.

7. Claims 6, 7, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al. (US 5,917,483) and Pasquali (US 6,535,882) as applied to claims 1, 9, 17, and 20 above, and further in view of Trask (US 6,249,355).

Claims 6 and 14:

Duncan and Pasquali fail to teach graphical data entry user interface being a check grid. Trask (US 6,249,355) teaches a graphical data entry user interface being a check grid (col. 7, lines 50 – 60). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine the graphical data entry user interface being a check grid taught by Trask with the logic control system disclosed by Duncan and Pasquali. Doing so enables the user to track various registers and bits within the various registers.

Claims 7 and 15:

Duncan and Pasquali fail to teach downloading said input control data table and said output data table to said programmable logic controller. Trask teaches

downloading said input control data table and said output data table to said programmable logic controller (col. 7, lines 24 – 36). It would have been obvious to one with ordinary skill in the art at the time of the invention to combine downloading said input control data table and said output data table to said programmable logic controller taught by Trask with the logic control system disclosed by Duncan and Pasquali. Doing so enables the user to track various registers and bits within the various registers.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J Joseph whose telephone number is 703-305-3917. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine Kincaid can be reached on 703-308-0640. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

November 14, 2003
tjj

STEVEN SAX
PRIMARY EXAMINER